AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims

Claim 1 (currently amended) Data access apparatus comprising:

an external memory unit for storing data, wherein the external memory unit has a second time ~~cycles~~ cycle for performing a task; and

a control unit couples with the external memory unit via a memory bus, comprising:

a microprocessor unit, having a first time ~~cycles~~ cycle to perform a microprocessor operating; and

a memory interface control unit for directing accessing data toward to a data address of the external memory unit, wherein the microprocessor unit could access data from the external memory via the memory interface control unit;

wherein the external memory unit has a data segment storing ~~a~~ flow control parameters and numerical arithmetic of the microprocessor operating, when the microprocessor unit is going to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit, an access request signal for accessing the data segment is directed to the external memory and the first time cycle is suspended until an acknowledge signal illustrative of the microprocessor unit may access the data segment of the external memory is received.

Claim 2 (currently amended) The data access apparatus according to claim 1, wherein the first time ~~cycles~~ cycle is ~~much~~ longer than the second time ~~cycles~~ cycle.

Claim 3 (currently amended) The data access apparatus according to claim 1, wherein the

first time cycle is revived from suspending when the second time cycle is finished. ~~when the microprocessor is going to access data from the data segment of the external memory unit, sending a access request signal and suspending the first time cycles until receiving an acknowledge signal, then reviving the first time cycles immediately.~~

Claim 4 (currently amended) The data access apparatus according to claim 3, wherein the duration ~~between~~ suspending ~~and reviving~~ the first time ~~cycles~~ cycle is ~~substantial~~ a time when ~~the second time cycles is finished, that is to say when~~ the external memory unit finishes a current task.

Claim 5 (original) The data access apparatus according to claim 1, wherein the external memory unit is a dynamic random access memory (DRAM).

Claim 6 (original) The data access apparatus according to claim 1, wherein a capacity of the data segment of the external memory unit is smaller than a capacity of the external memory unit.

Claim 7 (original) The data access apparatus according to claim 1, wherein the data access apparatus could be applied to an optical-electronic system and which is selected from: a CD-ROM, CD-RW, DVD+/-ROM, DVD+/-RW.

Claim 8 (currently amended) A control unit of data access with couples to an external memory unit, having a second time ~~cycles~~ cycle for performing a task, via a memory bus for an optical-electronic system, the control unit of data access comprising:
a memory interface control unit for directing accessing data toward to a data address of the external memory unit; and

a microprocessor having a first time ~~cycles~~ cycle to perform a microprocessor operation, wherein when the microprocessor is going to access data from the external memory unit via the memory interface, the control unit would send an access request signal to the external memory unit

wherein ~~data of~~ flow control parameters and numerical arithmetic of the microprocessor operating ~~which used to be stored in an internal memory unit of the control unit~~ is ~~replaced by~~ stored in a data segment within the external memory unit, when the microprocessor is going to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit, the access request signal for accessing the data segment is directed to the external memory and the first time cycle is suspended until an acknowledge signal illustrative of the microprocessor unit may access the data segment of the external memory is received.

Claim 9 (currently amended) The control unit of data access according to claim 8, wherein the first time ~~cycles~~ cycle is ~~much~~ longer than the second time ~~cycles~~ cycle.

Claim 10 (currently amended) The control unit of data access according to claim 8, wherein ~~when sending the access request signal, the first time cycles is suspended in the meantime until receiving a acknowledge signal, then the first time cycles is revived immediately~~ the first time cycle is revived from suspending when the second time cycle is finished.

Claim 11 (currently amended) The control unit of data access according to claim 10, wherein the duration between the first time ~~cycles~~ cycle suspended and revived is ~~substantial~~ a time ~~when the second time cycles is finished, that is to say~~ when the external memory unit finishes a current task.

Claim 12 (original) The control unit of data access according to claim 8, wherein the external memory unit is a DRAM.

Claim 13 (original) The control unit of data access according to claim 8, wherein a capacity of the data segment of the external memory unit is smaller than a capacity of the external memory unit.

Claim 14 (original) The control unit of data access according to claim 8, wherein the optical-electronic is selected from: a CD-ROM, a CD-RW, a DVD+/-ROM, and DVD+/-RW.

Claim 15 (currently amended) A data access method used in a control unit for accessing data in an external memory, comprising:

suspending a first time clock used by a microprocessor of the control unit when the microprocessor ~~sending~~ sends an access request signal for accessing a data segment in the external memory, wherein the data segment stores flow control parameters and numerical arithmetic of the microprocessor operating; and

reviving the first time clock when ~~receiving an acknowledgement signal~~ an acknowledge signal illustrative of the microprocessor may access the data segment of the external memory is received;

~~wherein data selected from: flow control parameters and numerical arithmetic is stored in a data segment of an external memory unit, and the first time cycles is a time for access data stored in the data segment.~~

Claim 16 (currently amended) The data access method according to claim 15, wherein the external memory unit has a second time ~~cycles~~ cycle which is ~~substantial~~ a time for ~~access~~ accessing data stored in the external memory unit.

Claim 17 (currently amended) The data access method according to claim 16, wherein ~~cycles of~~ the first time ~~cycles~~ cycle is ~~much~~ longer than ~~cycles of~~ the second time ~~cycles~~ cycle.

Claim 18 (currently amended) The data access method according to claim 16, wherein duration of the first time ~~cycles~~ cycle between being suspended and being revived is ~~substantial~~ a time of the second time ~~clock~~ cycle being finished.

Claim 19 (currently amended) The data access method according to claim 15, further comprising the external memory unit performs a current task when suspending the first time ~~cycles~~ cycle, and after finishing the current task, reviving the first time ~~cycles~~ cycle immediately.

Claim 20 (original) The data access method according to claim 15, wherein the method could be applied to an optical-electronic system which is selected from: a CD-ROM, a CD-RW, a DVD+/-ROM, and a DVD+/-RW.